CLAIMS

What is claimed is:

1. A method for forming polymer within a reaction chamber, the process comprising:

providing a reaction chamber;

introducing a polymer-forming gas within the reaction chamber; and

regulating an environment within the reaction chamber to form a polymer on an interior surface of the reaction chamber.

2. The method of claim 1, wherein a semiconductor wafer is present in the reaction chamber concurrent with the provision of the polymer-forming gas.

3. The method of claim 1, wherein a semiconductor wafer is not present in the reaction chamber concurrent with the provision of the polymer-forming gas.

4. The method of claim 1, wherein the environment within the reaction chamber comprises a temperature range between about 90°C and 250°C.

5. The method of claim 1, wherein the environment within the reaction chamber comprises a pressure range between about 0mT to about 200mT.

6. The method of claim 1, wherein the provided polymer-building gas comprises at least one of:

difluoromethane;

trifluoromethane;

octofluorocyclobutane; and

hexafluoro-13 butadiene.

7. The method of claim 1, wherein the reaction chamber comprises an etching chamber.

8. A method of manufacturing an integrated circuit, the method comprising the acts of:

disposing a semiconductor wafer in a reaction chamber;

processing the semiconductor wafer in the reaction chamber; and

providing a polymer-building gas in the reaction chamber to create a layer of polymer on an interior portion of the reaction chamber.

9. The method of claim 8, wherein the polymer-building gas is provided prior to disposing the semiconductor wafer in the reaction chamber.

10. The method of claim 8, wherein the polymer-building gas is provided during the processing of the semiconductor wafer in the reaction chamber.

11. The method of claim 8, wherein the provided polymer-building gas comprises at least one of:

difluoromethane;

trifluoromethane;

octofluorocyclobutane; and

hexafluoro-13 butadiene.

12. The method of claim 8, wherein the polymer-building gas is provided in a relatively small ratio as compared with a reactant gas.

13. The method of claim 8, wherein providing the polymer-building gas reduces the standard deviation of the critical dimensions of the semiconductor wafer.

14. The method of claim 8, wherein the semiconductor wafer disposed in the reaction chamber comprises a layered semiconductor wafer.

15. The method of claim 14, wherein at least one layer of the layered semiconductor wafer was formed through deposition.

16. The method of claim 14, wherein the layered semiconductor wafer comprises at least one of:

an oxide layer;

an anti-reflective coating; and

a photoresist layer.

17. The method of claim 8, wherein processing the semiconductor wafer in the reaction chamber comprises at least one of:

layering the semiconductor wafer; and

patterning the semiconductor wafer.

18. The method of claim 17, wherein layering the semiconductor wafer comprises at least one of:

depositing material on the semiconductor wafer; and

growing material on the semiconductor wafer.

19. The method of claim 17, wherein patterning the semiconductor wafer comprises etching at least one layer of the semiconductor wafer.

20. The method of claim 19, wherein etching at least one layer of the semiconductor wafer comprises etching a photoresist layer of the semiconductor wafer.

21. The method of claim 20, wherein etching the photoresist layer of the semiconductor wafer comprises plasma etching of the photoresist layer.

22. The method of claim 21, wherein the polymer-forming gas is provided concurrently with the plasma etching of the photoresist layer.

23. A method of manufacturing an electronic device, the method comprising:

providing an integrated circuit manufactured by a process comprising:

disposing a semiconductor wafer in a reaction chamber;

processing the semiconductor wafer in the reaction chamber; and

providing a polymer-building gas in the reaction chamber to create a layer of polymer on an interior portion of the reaction chamber;

packaging the integrated circuit; and

electrically coupling the integrated circuit to a substrate.

24. The method of claim 23, wherein a plurality of integrated circuits are electrically coupled to the substrate.

25. The method of claim 23, wherein the substrate comprises a circuit board.

26. The method of claim 23, wherein the electronic device comprises a memory device.

27. The method of claim 23, wherein the electronic device comprises a DIMM.

28. A method of manufacturing an electronic system, the method comprising:

providing an integrated circuit manufactured by a process comprising:

disposing a semiconductor wafer in a reaction chamber;

processing the semiconductor wafer in the reaction chamber; and

providing a polymer-building gas in the reaction chamber to create a layer of polymer on an interior portion of the reaction chamber; and

incorporating the integrated circuit into an electronic device.

29. The method of claim 28, wherein the electronic system comprises a processor based system.

30. The method of claim 29, wherein the processor based system comprises at least one of:

a computer;

a pager;

a cellular communication device;

a personal organizer; and

a control circuit.

31. The method of claim 28, wherein at least one peripheral device is attached to the electronic system.

32. The method of claim 31, wherein the at least one peripheral comprises at least one of:

a user interface;

a display; and

an antenna.